REMARKS

Favorable reconsideration of this application in view of the remarks to follow, and allowance of the claims of the present application, are respectfully requested.

In the Office Action dated March 20, 2006, Claims 1-9, and 19-20 are rejected under 35 U.S.C. §102(b) as anticipated by the disclosure of U.S. Patent No. 6,287,931 to Chen (hereinafter "Chen"). Specifically, the Examiner asserts that Chen teaches a semiconductor structure comprising a high performance metal stacked inductor, as claimed in the present application.

Applicants respectfully submit that Chen does not teach the claimed semiconductor structure recited in Claim 1. Specifically, Chen does not disclose a metal stacked inductor comprising at least one first layer of metal which serves as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal, wherein said first layer of metal is in electrical contact with a lower metal wire by a via, and said first layer of metal and said second layer of metal are not interconnected by a via.

It is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. *In re King*, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference.

Chen is directed to a method of fabricating an on-chip inductor over an insulating layer with low permitivity or high permeability so as to decrease both parasitic capacitance and mutual inductance. Specifically, Figures 2C, 2D, and 4 and the specification of Chen (column 3, line 35 to column 4, line 37) clearly indicate a tri-metal stacked inductor wherein the three metal layers, i.e., layers 24, 28, and 32, are interconnected through vias 27 and 31. In contrast, the first

metal layer and the second metal layer in the claimed semiconductor structure are not interconnected by a via. (see Claim 1, Figures 2, 3, and 4E, and paragraph [0018] on page 3).

The Examiner points to Column 4, lines 38-47 and Figure 2D of Chen asserting that Chen discloses a multiple-metal stacked inductor wherein the different layers of metal are not interconnected by a via. Applicants respectfully disagree with the Examiner for the following reasons.

First, it is known in the art that a mere recitation of stacking metal layers does not refer to a multiple-metal stacked structure wherein the different layers of metal are not interconnected by a via. To the contrary, one skilled in the art would readily understand that a bare assertion of a multiple-metal stacked inductor without any specific showing, as Chen does, denotes metal layers that are placed on top of each other through via connections.

Second, the disclosure of Chen as a whole does not disclose or recognize a stacking metal structure wherein different layers of metal are not interconnected by a via. As indicated in Figures 2C, 2D, and 4 and the specification of Chen (column 3, line 35 to column 4, line 37), the on-chip inductor disclosed in Chen comprises a stacking metal structure wherein the three metal layers, i.e., layers 24, 28, and 32, are interconnected through vias 27 and 31. Although Chen recites that "two or more metal layers can be stacked to implement the spiral conductive layer 28 to further lower series resistance Rs and thus increase the quality factor of the fabricated inductor," Chen is completely silent as to whether vias are used to connect the multiple metal layers. It is well known in the art that the direct current resistance of a metal line that forms a spiral inductor is a major contributor to the inductor Q degradation (See U.S. Patent No. 5,446,311 to Ewen et al., which is attached herein as Exhibit 1). It has also been taught that multiple metalization levels can be used to reduce the inductor resistance (See U.S. Patent No.

5,446,311 to Ewen et al., which is attached herein as Exhibit 1). In view of the disclosure of Chen as a whole and the state of general knowledge in the art, applicants submit that the recitation of stacking metal layers in Chen does not disclose stacking metal layers wherein the metal layers are not connected by vias. Instead, Chen merely discloses a multiple-metal stacked inductor wherein the different layers of metal are interconnected by vias, as disclosed in Figure 3 of U.S. Patent No. 5,446,311 to Ewen et al., which is attached herein as Exhibit 1. It is important to note that the present application explicitly claims a semiconductor structure wherein the first layer of metal and the second layer of metal are not interconnected by a via.

Since Chen fails to disclose an essential feature of the claimed semiconductor structure, Claims 1-9, and 19-20 are not anticipated by the disclosure of Chen. The §102(b) rejection has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Claims 10 and 13 are rejected under 35 U.S.C. §103(a) as unpatentable over Chen in view of U.S. Patent No. 6,639,298 to Chaudhry et al. (hereinafter "Chaudhry et al."). Claims 11-12 and 14-15 are rejected under 35 U.S.C. §103(a) as unpatentable over Chen in view of U.S. Patent Application Publication No. 2002/0125575 to Chaen (hereinafter "Chaen"). Claims 16 is rejected under 35 U.S.C. §103(a) as unpatentable over Chen and Chaen in view of U.S. Patent No. 6,395,637 to Park et al. (hereinafter "Park et al."). Claim 17 is rejected under 35 U.S.C. §103(a) as unpatentable over Chen in view of Park et al. Claims 18 is rejected under 35 U.S.C. §103(a) as unpatentable over Chen and Chaudhry et al. in view of Park et al.

Applicants respectfully submit that the present invention is not rendered obvious by the disclosures of the applied references because the applied references, solely or in combination, do not disclose, suggest, or recognize applicants'claimed semiconductor structure.

Specifically, the applied references, solely or in combination, do not teach or suggest the claimed metal stacked inductor comprising at least one first layer of metal which serves as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal, wherein said first layer of metal is in electrical contact with a lower metal wire by a via, and said first layer of metal and said second layer of metal are not interconnected by a via.

As discussed previously, Chen fails to disclose a semiconductor structure wherein the first layer of metal and the second layer of metal are not interconnected by a via. Chaudhry, discloses an integrated circuit inductor having a plurality of insulating layers and a plurality of metallization layers, which differs considerably from the claimed metal stacked inductor. Chaen discloses an inductor comprising a plurality of metal layers stacked on a first insulating layer, but the lower-most metal layer 6 does not serve as wiring levels as in the claimed structure. Park emphasizes that the high performance of the inductor is achieved by fully filling the via hole and the via recesses with the Al layer to increase the actual thickness of the inductor coil (lines 9-21, column 6), while the present application specifically claims that the second layer of metal and the first layer of the metal are not interconnected by a via.

The §103 rejection also fails because there is no motivation in the applied references which suggests modifying the disclosed devices to achieve the claimed semiconductor structure. As discussed previously, Chen is completely silent as to whether vias are used to connect the multiple metal layers. While Chaen states that the semiconductor structure disclosed therein is intended to prevent collapse and delamination of an inductor without increasing an occupied area or to further reduce the area of the inductor while (paragraph [0011] of Chaen), Chaudhry specifically teaches that the desirable low-resistance (and thus high Q) of the inductors

is achieved by using a dual damascene process to form such an inductor (lines 56-67, Column 2 of Chaudhry). Notably, the present specification states that the high performance of the claimed inventive inductor having substantially low sheet resistance is achieved because no via is used interconnecting the multiple layers of metal (paragraphs [0018] and [0019] of the specification). As discussed previously, Park emphasizes the use of vias to achieve high performance of the disclosed inductor. That is, Park teaches away from the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification suggested by the Examiner. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Vaeck*, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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Enclosure (Exhibit 1)